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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

μPD720114

ECOUSB™ Series

USB 2.0 HUB CONTROLLER

The μPD720114 is a USB 2.0 hub device that complies with the Universal Serial Bus (USB) Specification Revision 2.0 and works up to 480 Mbps. USB 2.0 compliant transceivers are integrated for upstream and all downstream ports. The μPD720114 works backward compatible either when any one of the downstream ports is connected to a USB 1.1 compliant device, or when the upstream port is connected to a USB 1.1 compliant host.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.
μPD720114 User's Manual: S17463E

FEATURES

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 1.5/12/480 Mbps)
- High-speed or full-speed packet protocol sequencer for Endpoint 0/1
- 4 (Max.) downstream facing ports
- Low power consumption (10 μA when hub in idle status, 149 mA when all parts run in HS mode)
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction.
- Supports split transaction to handle full-speed and low-speed transaction on downstream facing ports when Hub controller is working in high-speed mode.
- One Transaction Translator per Hub and supports four non-periodic buffers
- Supports self-powered and bus-powered mode
- Supports individual or global over-current detection and individual or ganged power control
- Supports downstream port status with LED
- Supports non-removable devices by I/O pin configuration
- Support Energy Star for PC peripheral system
- On chip Rpu, Rpd resistors and regulator (for core logic)
- Use 30 MHz crystal
- 3.3 V power supply

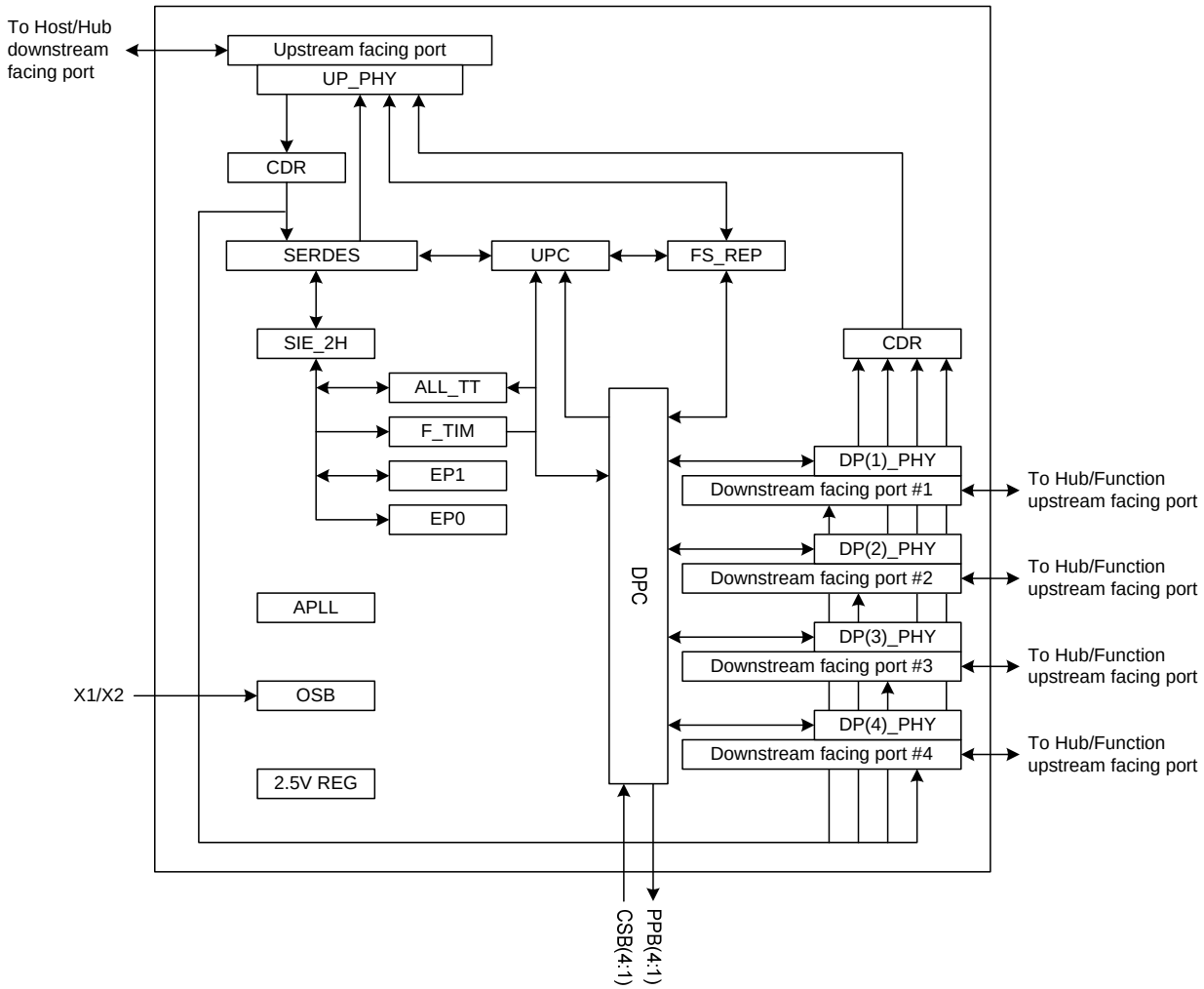
Document No. S17462EJ6V0DS00 (6th edition)
Date Published December 2009 NS
Printed in Japan

The mark "<R>" shows major revised points.

ORDERING INFORMATION

Part Number	Package	Remark
μPD720114GA-9EU-A	48-pin plastic TQFP (Fine pitch) (7 × 7)	Lead-free product
μPD720114GA-YEU-A	48-pin plastic TQFP (Fine pitch) (7 × 7)	Lead-free product
<R> μPD720114K9-4E4-A	40-pin plastic QFN (6 × 6)	Lead-free product

BLOCK DIAGRAM

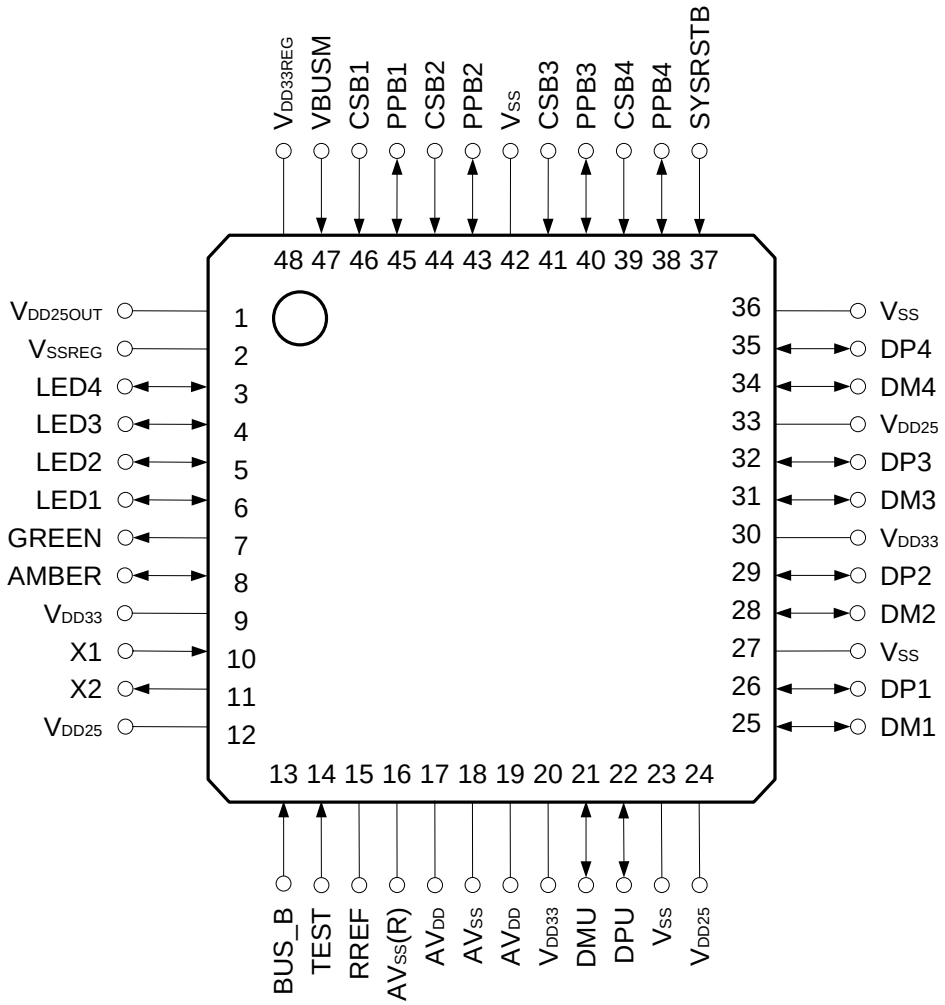


APLL	:	Generates all clocks of Hub.
ALL_TT	:	Translates the high-speed transactions (split transactions) for full/low-speed device to full/low-speed transactions. ALL_TT buffers the data transfer from either upstream or downstream direction. For OUT transaction, ALL_TT buffers data from upstream port and sends it out to the downstream facing ports after speed conversion from high-speed to full/low-speed. For IN transaction, ALL_TT buffers data from downstream ports and sends it out to the upstream facing ports after speed conversion from full/low-speed to high-speed.
CDR	:	Data & clock recovery circuit
DPC	:	Downstream Port Controller handles Port Reset, Enable, Disable, Suspend and Resume
DP(n)_PHY	:	Downstream transceiver supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction
EP0	:	Endpoint 0 controller
EP1	:	Endpoint 1 controller
F_TIM (Frame Timer)	:	Manages hub's synchronization by using micro-SOF which is received at upstream port, and generates SOF packet when full/low-speed device is attached to downstream facing port.
FS_REP	:	Full/low-speed repeater is enabled when the μPD720114 are worked at full-speed mode
OSB	:	Oscillator Block
2.5V REG	:	On chip 2.5V regulator
SERDES	:	Serializer and Deserializer
SIE_2H	:	Serial Interface Engine (SIE) controls USB2.0 and 1.1 protocol sequencer.
UP_PHY	:	Upstream Transceiver supports high-speed (480 Mbps), full-speed (12 Mbps) transaction
UPC	:	Upstream Port Controller handles Suspend and Resume

PIN CONFIGURATION (TOP VIEW)

- **48-pin plastic TQFP (Fine pitch) (7 × 7)**

  μPD720114GA-9EU-A
  μPD720114GA-YEU-A

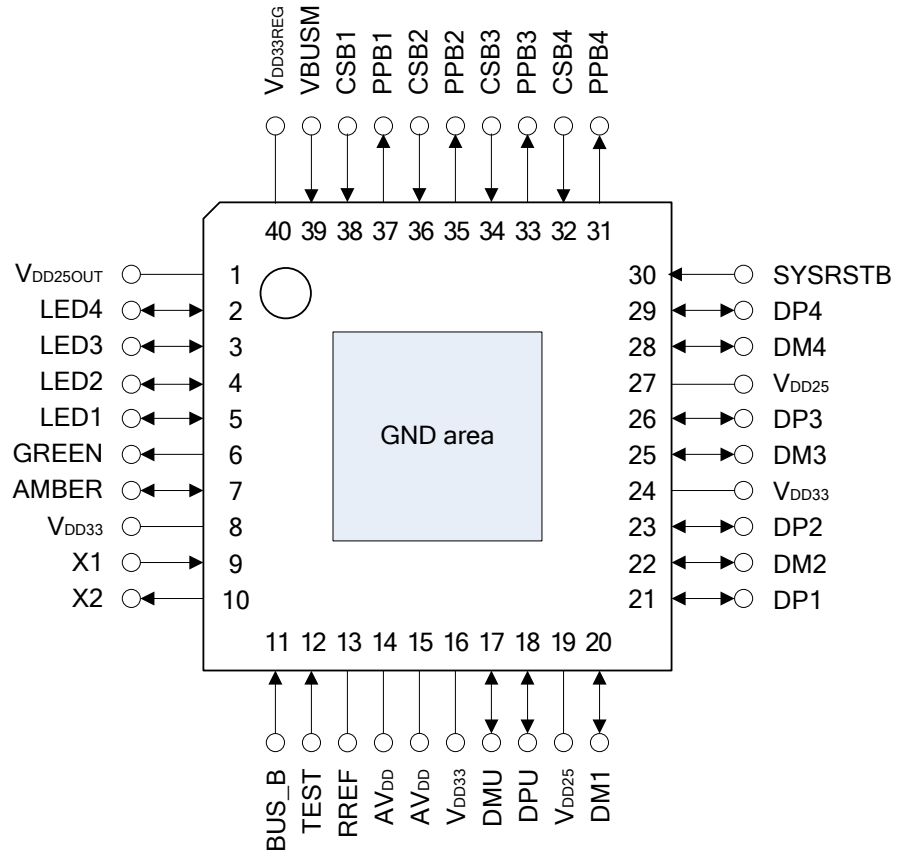


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	$V_{DD25OUT}$	13	BUS_B	25	DM1	37	SYSRSTB
2	V_{SSREG}	14	TEST	26	DP1	38	PPB4
3	LED4	15	RREF	27	V_{SS}	39	CSB4
4	LED3	16	AV_{SS}(R)	28	DM2	40	PPB3
5	LED2	17	AV_{DD}	29	DP2	41	CSB3
6	LED1	18	AV_{SS}	30	V_{DD33}	42	V_{SS}
7	GREEN	19	AV_{DD}	31	DM3	43	PPB2
8	AMBER	20	V_{DD33}	32	DP3	44	CSB2
9	V_{DD33}	21	DMU	33	V_{DD25}	45	PPB1
10	X1	22	DPU	34	DM4	46	CSB1
11	X2	23	V_{SS}	35	DP4	47	VBUSM
12	V_{DD25}	24	V_{DD25}	36	V_{SS}	48	$V_{DD33REG}$

Remark AV_{SS}(R) should be used to connect RREF through 1 % precision reference resistor of 2.43 kΩ.

<R> • **40-pin plastic QFN (6 × 6)**

μPD720114K9-4E4-A



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	$V_{DD25OUT}$	11	BUS_B	21	DP1	31	PPB4
2	LED4	12	TEST	22	DM2	32	CSB4
3	LED3	13	RREF	23	DP2	33	PPB3
4	LED2	14	AV_{DD}	24	V_{DD33}	34	CSB3
5	LED1	15	AV_{DD}	25	DM3	35	PPB2
6	GREEN	16	V_{DD33}	26	DP3	36	CSB2
7	AMBER	17	DMU	27	V_{DD25}	37	PPB1
8	V_{DD33}	18	DPU	28	DM4	38	CSB1
9	X1	19	V_{DD25}	29	DP4	39	VBUSM
10	X2	20	DM1	30	SYSRSTB	40	$V_{DD33REG}$

Remark RREF should be connected to ground through 1% precision reference resistor of 2.43 kΩ.

1. PIN INFORMATION

Pin Name	I/O	Buffer Type	Active Level	Function
X1	I	2.5 V input		30 MHz Crystal oscillator in
X2	O	2.5 V output		30 MHz Crystal oscillator out
SYSRSTB	I	3.3 V Schmitt input	Low	Asynchronous chip hardware reset
DP(4:1)	I/O	USB D+ signal I/O		USB's downstream facing port D+ signal
DM(4:1)	I/O	USB D− signal I/O		USB's downstream facing port D− signal
DPU	I/O	USB D+ signal I/O		USB's upstream facing port D+ signal
DMU	I/O	USB D− signal I/O		USB's upstream facing port D− signal
BUS_B	I	3.3 V Schmitt input		Power mode select
RREF	A (O)	Analog		Reference resistor connection
CSB1	I	5 V tolerant Schmitt input	Low	Port's over-current status input.
CSB(4:2)	I	3.3 V Schmitt input	Low	Port's over-current status input
PPB(4:1)	I/O	3.3 V output / input	Low	Port's power supply control output or hub configuration input
VBUSM	I	5 V tolerant Schmitt input		Upstream V_{BUS} monitor
AMBER	I/O	3.3V output / input		Amber colored LED control output or port indicator select
GREEN	O	3.3V output		Green colored LED control output or port indicator select
LED(4:1)	I/O	3.3V output / input	Low	LED indicator output show downstream port status or Removable/Non-removable select
TEST	I	3.3 V Schmitt input		Test signal
$V_{DD25OUT}$				On chip 2.5 V regulator output, it must have a 22 μF (or greater) capacitor to V_{SSREG}
V_{DD33}				3.3 V V_{DD}
$V_{DD33REG}$				3.3 V V_{DD} for on chip 2.5 V regulator input, it must have a 4.7 μF (or greater) capacitor to V_{SSREG}
V_{DD25}				2.5 V V_{DD}. These pins must be supplied from $V_{DD25OUT}$, output from internal regulator
AV_{DD}				2.5 V V_{DD} for analog circuit
V_{SS}				V_{SS}
V_{SSREG}				On chip 2.5 V regulator V_{SS}
AV_{SS}				V_{SS} for analog circuit
AV_{SS}(R)				V_{SS} for reference resistor, Connect to AV_{SS}.

Remark "5 V tolerant" means that the buffer is 3 V buffer with 5 V tolerant circuit.

2. ELECTRICAL SPECIFICATIONS

2.1 Buffer List

- 2.5 V Oscillator interface
  X1, X2
- 5 V tolerant Schmitt input buffer
  CSB1, VBUSM
- 3.3 V Schmitt input buffer
  CSB(4:2),BUS_B, SYSRSTB, TEST
- 3.3 V I_{OL} = 12 mA output buffer
  GREEN
- 3.3 V input and 3.3 V I_{OL} = 3 mA output buffer
  PPB(4:1), LED(4:1)
- 3.3 V input and I_{OL} = 12 mA output buffer
  AMBER
- USB2.0 interface
  DPU, DMU, DP(4:1), DM(4:1), RREF

Above, “5 V” refers to a 3 V input buffer that is 5 V tolerant (has 5 V maximum input voltage). Therefore, it is possible to have a 5 V connection for an external bus.

2.2 Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, $V_{DD33REG}$	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, $V_{DD33REG}$	Indicates the voltage range for normal logic operations to occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, applied to the input pins of the device, which indicates the high level state for normal operation of the input buffer. * If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, applied to the input pins of the device, which indicates the low level state for normal operation of the input buffer. * If a voltage that is equal to or less than the “Max.” value is applied, the input voltage is guaranteed as low level voltage.
Hysteresis voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t_{ri}	Indicates allowable input rise time to input signal transition time from $0.1 \times V_{DD}$ to $0.9 \times V_{DD}$.
Input fall time	t_{fi}	Indicates allowable input fall time to input signal transition time from $0.9 \times V_{DD}$ to $0.1 \times V_{DD}$.

Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows into a 3-state output pin when it is in a high-impedance state and a voltage is applied to the pin.
Output short circuit current	I_{OS}	Indicates the current that flows from an output pin when it is shorted to GND pins.
Input leakage current	I_I	Indicates the current that flows into an input pin when a voltage is applied to the pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that can flow out of an output pin in the high-level state without reducing the output voltage below the specified V_{OH}. (A negative current indicates current flowing out of the pin.)

2.3 Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD33}, $V_{DD33REG}$		−0.5 to +4.6	V
Input/output voltage	V_I/V_O			
3.3 V input/output voltage		3.0 V ≤ V_{DD33} ≤ 3.6 V V_I/V_O < V_{DD33} + 1.0 V	−0.5 to +4.6	V
5 V input/out voltage		3.0 V ≤ V_{DD33} ≤ 3.6 V V_I/V_O < V_{DD33} + 3.0 V	−0.5 to +6.6	V
Output current	I_O	I_{OL} = 3 mA I_{OL} = 12 mA	10 40	mA mA
Operating temperature	T_A		0 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD33}, $V_{DD33REG}$	3.3 V for V_{DD33} pins	3.14	3.30	3.46	V
High-level input voltage	V_{IH}					
3.3 V High-level input voltage			2.0		V_{DD33}	V
5.0 V High-level input voltage			2.0		5.5	V
Low-level input voltage	V_{IL}					
3.3 V Low-level input voltage			0		0.8	V
5.0 V Low-level input voltage			0		0.8	V
Hysteresis voltage	V_H					
5 V Hysteresis voltage			0.3		1.5	V
3.3 V Hysteresis voltage			0.2		1.0	V
Input rise time for SYSRSTB	t_{rst}				10	ms
Input rise time	t_{ri}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms
Input fall time	t_{fi}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms

DC Characteristics (V_{DD33} = 3.14 to 3.46 V, T_A = 0 to +70 °C)

Control Pin Block

Parameter	Symbol	Condition	Min.	Max.	Unit
Off-state output leakage current	I_{OZ}	$V_O = V_{DD33}$, V_{DD25} or V_{SS}		±10	μA
Output short circuit current	I_{OS} Note			−250	mA
Low-level output current	I_{OL}				
3.3 V low-level output current (3 mA)		V_{OL} = 0.4 V	3		mA
3.3 V low-level output current (12 mA)		V_{OL} = 0.4 V	12		mA
High-level output current	I_{OH}				
3.3 V high-level output current (3 mA)		V_{OH} = 2.4 V	−3		mA
3.3 V high-level output current (12 mA)		V_{OH} = 2.4 V	−12		mA
Input leakage current	I_I				
3.3 V buffer		$V_I = V_{DD}$ or V_{SS}		±10	μA
5.0 V buffer		$V_I = V_{DD}$ or V_{SS}		±10	μA

Note The output short circuit time is measured at one second or less and is tested with only one pin on the LSI.

USB Interface Block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Output pin impedance	Z_{HSDRV}	Includes R_S resistor	40.5	49.5	Ω
Termination voltage for upstream facing port pullup (full-speed)	V_{TERM}		3.0	3.6	V
Input Levels for Low-/full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	V
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	$\lvert(D+) - (D-)\rvert$	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Low-/full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		−50	+500	mV
High-speed differential input signaling levels	See **Figure 2-4**.				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		−10.0	+10	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		−10.0	+10	mV
Chirp J level (different signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (different signal)	V_{CHIRPK}		−900	−500	mV

Figure 2-1. Differential Input Sensitivity Range for Low-/full-speed

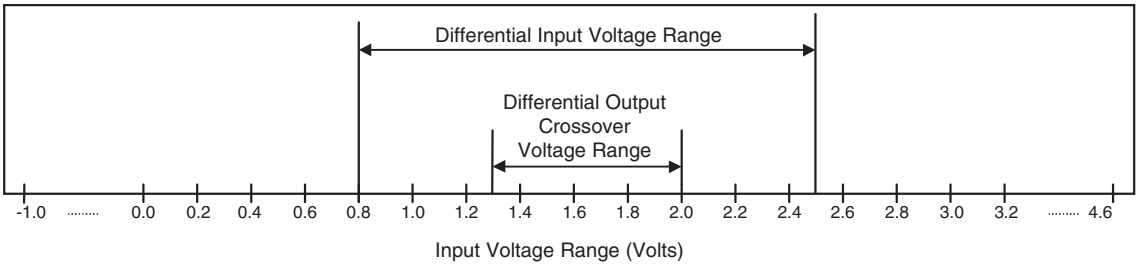


Figure 2-2. Full-speed Buffer V_{OH}/I_{OH} Characteristics for High-speed Capable Transceiver

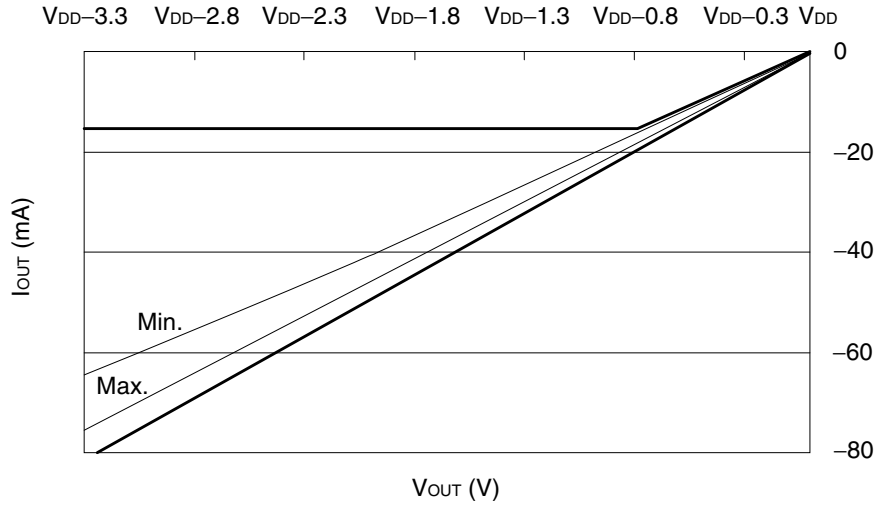


Figure 2-3. Full-speed Buffer V_{OL}/I_{OL} Characteristics for High-speed Capable Transceiver

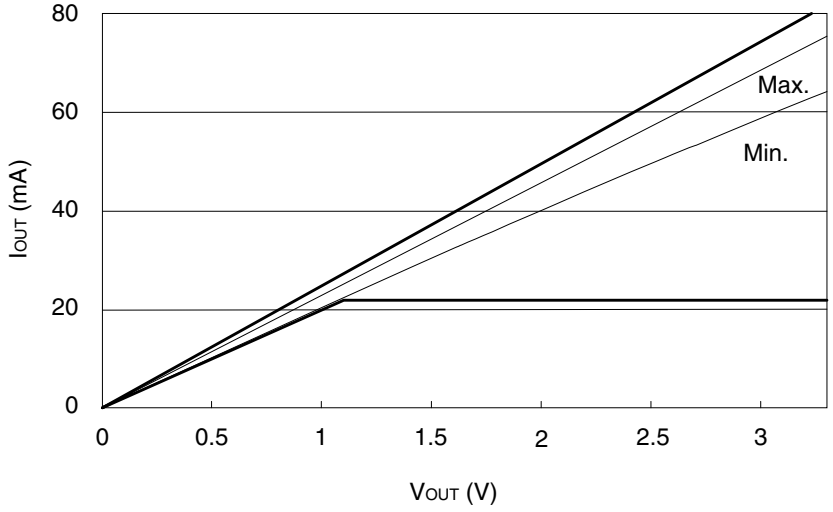


Figure 2-4. Receiver Sensitivity for Transceiver at DP/DM

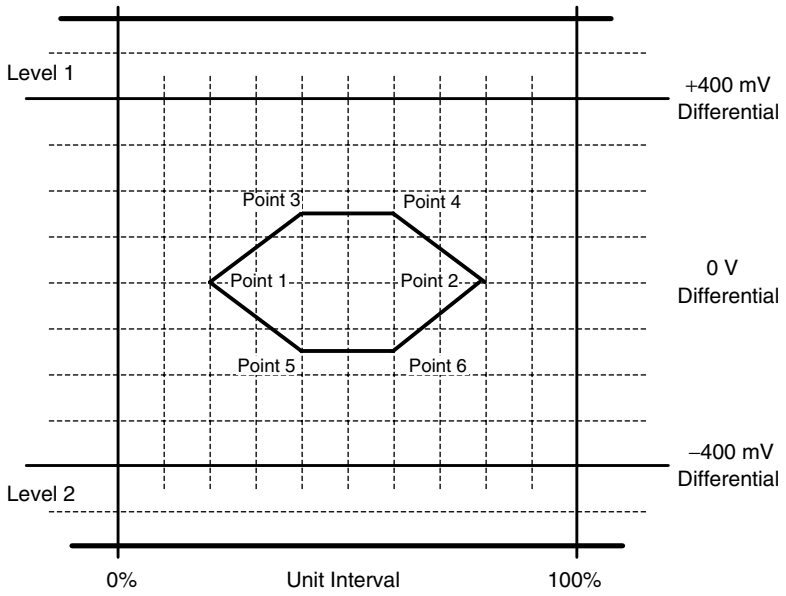
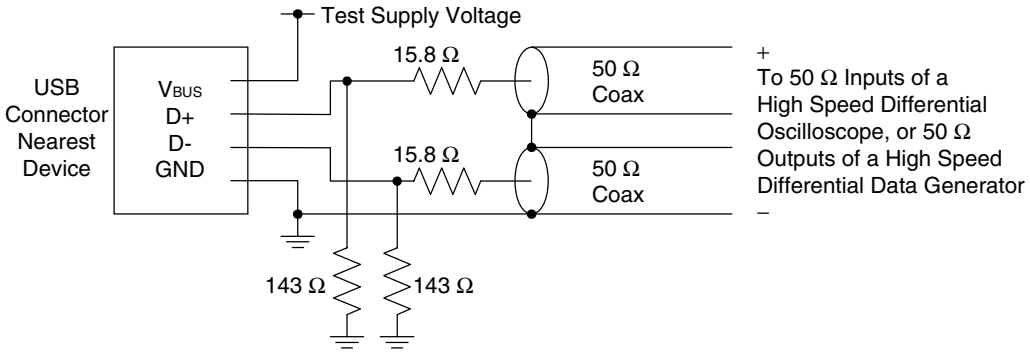


Figure 2-5. Receiver Measurement Fixtures



Power Consumption

Parameter	Symbol	Condition	Typ.	Unit
Power Consumption	P_{W-0}	The power consumption under the state without suspend. All the ports do not connect to any function. Note 1		
		Hub controller is operating at full-speed mode.	31	mA
		Hub controller is operating at high-speed mode.	86	mA
	P_{W-2}	The power consumption under the state without suspend. The number of active ports is 2. Note 2		
		Hub controller is operating at full-speed mode.	36	mA
		Hub controller is operating at high-speed mode.	120	mA
	P_{W-3}	The power consumption under the state without suspend. The number of active ports is 3. Note 2		
		Hub controller is operating at full-speed mode.	38	mA
		Hub controller is operating at high-speed mode.	134	mA
	P_{W-4}	The power consumption under the state without suspend. The number of active ports is 4. Note 2		
		Hub controller is operating at full-speed mode.	41	mA
		Hub controller is operating at high-speed mode.	149	mA
	P_{W-UNP}	The power consumption under unplug and the hub in idle state. Note 3	10	μA
	P_{W_S}	The power consumption under plug (V_{BUS} ON) and the hub in suspend state. Note 4	220	μA

Notes 1. Ports available but inactive or unplugged do not add to the power consumption.

2. The power consumption depends on the number of ports available and actively operating.

3. If the μPD720114 is locally powered and the upstream facing port is unplugged, μPD720114 goes into suspend state and downstream facing port V_{BUS} goes down.

4. If the upstream V_{BUS} in OFF state, the power consumption is same as P_{W-UNP}.

AC Characteristics (V_{DD33} = 3.14 to 3.46 V, T_A = 0 to +70 °C)

Pin capacitance

Parameter	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_I	V_{DD} = 0 V, T_A = 25 °C		6	pF
Output capacitance	C_O	f_C = 1 MHz		6	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		6	pF

System Clock Ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	f_{CLK}	Crystal	−500 ppm	30	+500 ppm	MHz
Clock Duty cycle	t_{DUTY}		40	50	60	%

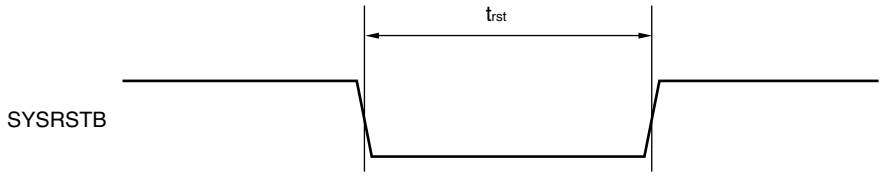
Remarks 1. Recommended accuracy of clock frequency is ± 100 ppm.

2. Required accuracy of X'tal is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

System Reset Timing

Parameter	Symbol	Conditions	Min.	Max.	Unit
Reset active time (**Figure 2-6**)	t_{rst}		5		μs

Figure 2-6. System Reset Timing



Over-current Response Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Over-current response time from CSB low to PPB high (**Figure 2-7**)	t_{OC}		4		5	ms

Figure 2-7. Over-current Response Timing

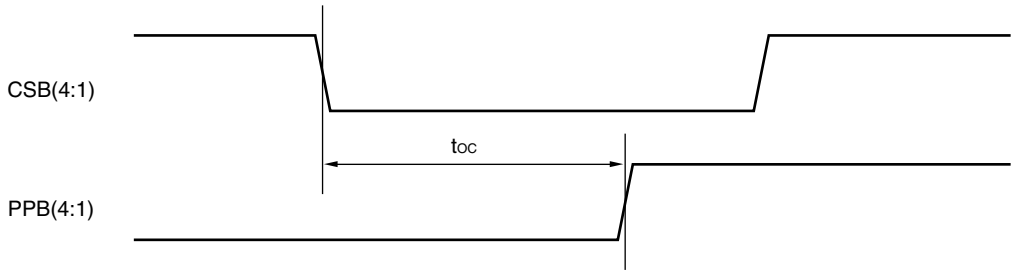
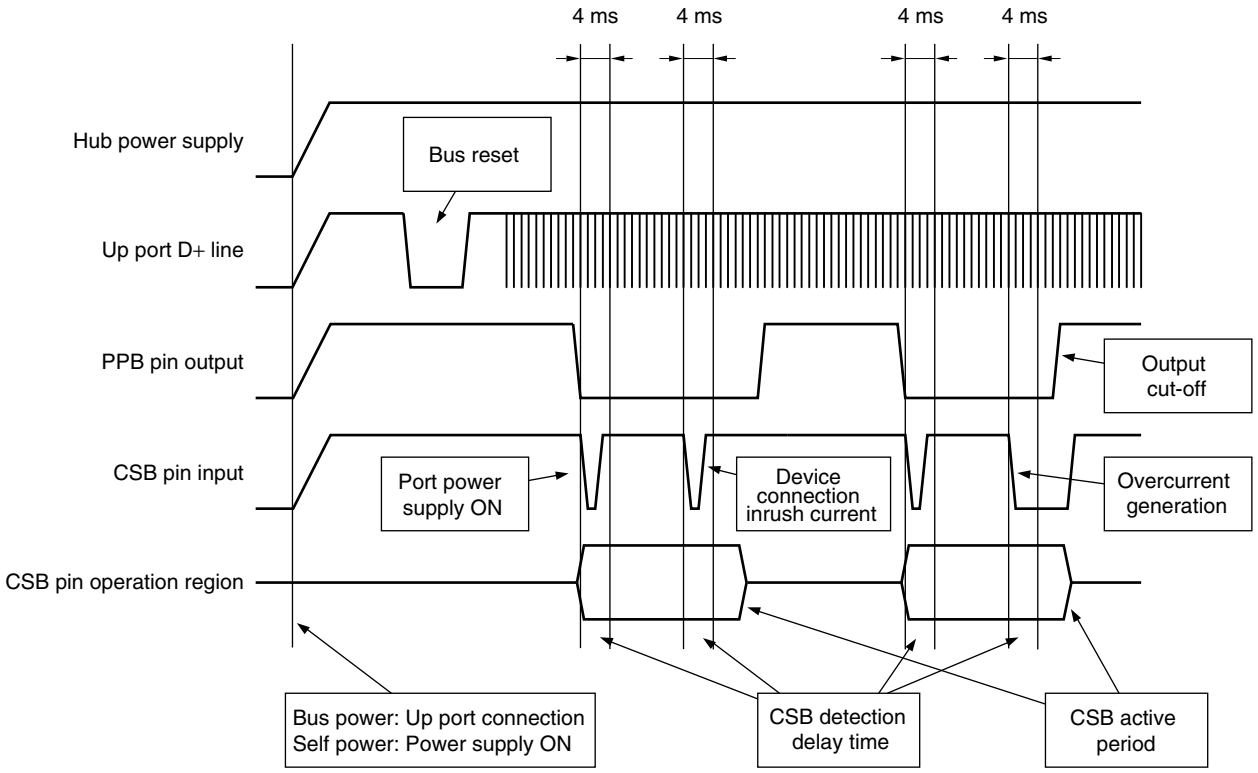


Figure 2-8. CSB/PPB Timing



Remark The active period of the CSB pin is in effect only when the PPB pin is ON.
There is a delay time of approximately 4 ms duration at the CSB pin.

USB Interface Block

(1/4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Low-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{LR}	C_L = 200 pF to 600 pF	75	300	ns
Fall time (90% to 10%)	t_{LF}	C_L = 200 pF to 600 pF	75	300	ns
Differential rise and fall time matching	t_{LRFM}	(t_{LR}/t_{LF}) Note	80	125	%
Low-speed data rate	$t_{LDRATHS}$	Average bit rate	1.49925	1.50075	Mbps
Downstream facing port source jitter total (including frequency tolerance) (**Figure 2-13**):					
To next transition	t_{DDJ1}		−25	+25	ns
For paired transitions	t_{DDJ2}		−14	+14	ns
Downstream facing port differential receiver jitter total (including frequency tolerance) (**Figure 2-15**):					
To next transition	t_{UJR1}		−152	+152	ns
For paired transitions	t_{UJR2}		−200	+200	ns
Source SE0 interval of EOP (**Figure 2-14**)	t_{LEOPT}		1.25	1.5	μs
Receiver SE0 interval of EOP (**Figure 2-14**)	t_{LEOPR}		670		ns
Width of SE0 interval during differential transition	t_{LST}			210	ns
Hub differential data delay (**Figure 2-11**)	t_{LHDD}			300	ns
Hub differential driver jitter (including cable) (**Figure 2-11**):					
Downstream facing port					
To next transition	t_{LDHJ1}		−45	+45	ns
For paired transitions	t_{LDHJ2}		−15	+15	ns
Upstream facing port					
To next transition	t_{LUHJ1}		−45	+45	ns
For paired transitions	t_{LUHJ2}		−45	+45	ns
Data bit width distortion after SOP (**Figure 2-11**)	t_{LSOP}		−60	+60	ns
Hub EOP delay relative to t_{HDD} (**Figure 2-12**)	t_{LEOPD}		0	200	ns
Hub EOP output width skew (**Figure 2-12**)	t_{LHESK}		−300	+300	ns
Full-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time (90% to 10%)	t_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms

Note Excluding the first transition from the Idle state.

(2/4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Full-speed Electrical Characteristics (Continued)					
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance) (**Figure 2-13**):		**Note**			
To next transition	t_{DJ1}		−3.5	+3.5	ns
For paired transitions	t_{DJ2}		−4.0	+4.0	ns
Source jitter for differential transition to SE0 transition (**Figure 2-14**)	t_{FDEOP}		−2	+5	ns
Receiver jitter (**Figure 2-15**):					
To Next Transition	t_{JR1}		−18.5	+18.5	ns
For Paired Transitions	t_{JR2}		−9	+9	ns
Source SE0 interval of EOP (**Figure 2-14**)	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP (**Figure 2-14**)	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns
Hub differential data delay (**Figure 2-11**)					
(with cable)	t_{HDD1}			70	ns
(without cable)	t_{HDD2}			44	ns
Hub differential driver jitter (including cable) (**Figure 2-11**):					
To next transition	t_{HDJ1}		−3	+3	ns
For paired transitions	t_{HDJ2}		−1	+1	ns
Data bit width distortion after SOP (**Figure 2-11**)	t_{FSOP}		−5	+5	ns
Hub EOP delay relative to t_{HDD} (**Figure 2-12**)	t_{FEOPD}		0	15	ns
Hub EOP output width skew (**Figure 2-12**)	t_{FHESK}		−15	+15	ns
High-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{HSR}		500		ps
Fall time (90% to 10%)	t_{HSF}		500		ps
Driver waveform	See **Figure 2-9**.				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 high-speed	Bit times
Data source jitter	See **Figure 2-9**.				
Receiver jitter tolerance	See **Figure 2-4**.				
Hub data delay (without cable)	t_{HSHDD}			36 high-speed+4 ns	Bit times
Hub data jitter	See **Figure 2-4**, **Figure 2-9**.				
Hub delay variation range	t_{HSHDV}			5 high-speed	Bit times

Note Excluding the first transition from the Idle state.

(3/4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Hub Event Timings					
Time to detect a downstream facing port connect event (**Figure 2-17**): Awake hub Suspended hub	t_{DCNN}		 2.5 2.5	 2000 12000	 μs μs
Time to detect a disconnect event at a hub's downstream facing port (**Figure 2-16**)	t_{DDIS}		2.0	2.5	μs
Duration of driving resume to a downstream port (only from a controlling hub)	t_{DRSMDN}		20		ms
Time from detecting downstream resume to rebroadcast	t_{URSM}			1.0	ms
Duration of driving reset to a downstream facing port (**Figure 2-18**)	t_{DRST}	Only for a SetPortFeature (PORT_RESET) request	10	20	ms
Time to detect a long K from upstream	t_{URLK}		2.5	100	μs
Time to detect a long SE0 from upstream	t_{URLSE0}		2.5	10000	μs
Duration of repeating SE0 upstream (for low-/full-speed repeater)	t_{URPSE0}			23	FS Bit times
Inter-packet delay (for high-speed) of packets traveling in same direction	$t_{HSIPDSD}$		88		Bit times
Inter-packet delay (for high-speed) of packets traveling in opposite direction	$t_{HSIPDOD}$		8		Bit times
Inter-packet delay for device/root hub response with detachable cable for high-speed	$t_{HSRSPIPD1}$			192	Bit times
Time of which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	t_{FILT}		2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence	t_{WTDCH}			100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset	t_{DCHBIT}		40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	t_{DCHSE0}		100	500	μs
Time from internal power good to device pulling D+ beyond V_{IHZ} (**Figure 2-18**)	t_{SIGATT}			100	ms
Debounce interval provided by USB system software after attach (**Figure 2-18**)	t_{ATTDB}			100	ms
Maximum duration of suspend averaging interval	$t_{SUSAVGI}$			1	s
Period of idle bus before device can initiate resume	t_{WTRSM}		5		ms
Duration of driving resume upstream	t_{DRSMUP}		1	15	ms

(4/4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Hub Event Timings (Continued)					
Resume recovery time	t_{RSMRCY}	Remote-wakeup is enabled	10		ms
Time to detect a reset from upstream for non high-speed capable devices	t_{DETRST}		2.5	10000	μs
Reset recovery time (**Figure 2-18**)	t_{RSTRCY}			10	ms
Inter-packet delay for full-speed	t_{IPD}		2		Bit times
Inter-packet delay for device response with detachable cable for full-speed	$t_{RSPIPD1}$			6.5	Bit times
SetAddress() completion time	$t_{DSETADDR}$			50	ms
Time to complete standard request with no data	$t_{DRQCMPLTND}$			50	ms
Time to deliver first and subsequent (except last) data for standard request	$t_{DRETDATA1}$			500	ms
Time to deliver last data for standard request	$t_{DRETDATAN}$			50	ms
Time for which a suspended hub will see a continuous SE0 on upstream before beginning the high-speed detection handshake	$t_{FILTSE0}$		2.5		μs
Time a hub operating in non-suspended full-speed will wait after start of SE0 on upstream before beginning the high-speed detection handshake	$t_{WTRSTFS}$		2.5	3000	ms
Time a hub operating in high-speed will wait after start of SE0 on upstream before reverting to full-speed	t_{WTREV}		3.0	3.125	ms
Time a hub will wait after reverting to full-speed before sampling the bus state on upstream and beginning the high-speed will wait after start of SE0 on upstream before reverting to full-speed	$t_{WTRSTHS}$		100	875	ms
Minimum duration of a Chirp K on upstream from a hub within the reset protocol	t_{UCH}		1.0		ms
Time after start of SE0 on upstream by which a hub will complete its Chirp K within the reset protocol	t_{UCHEND}			7.0	ms
Time between detection of downstream chip and entering high-speed state	t_{WTHS}			500	μs
Time after end of upstream Chirp at which hub reverts to full-speed default state if no downstream Chirp is detected	t_{WTFS}		1.0	2.5	ms

Figure 2-9. Transmit Waveform for Transceiver at DP/DM

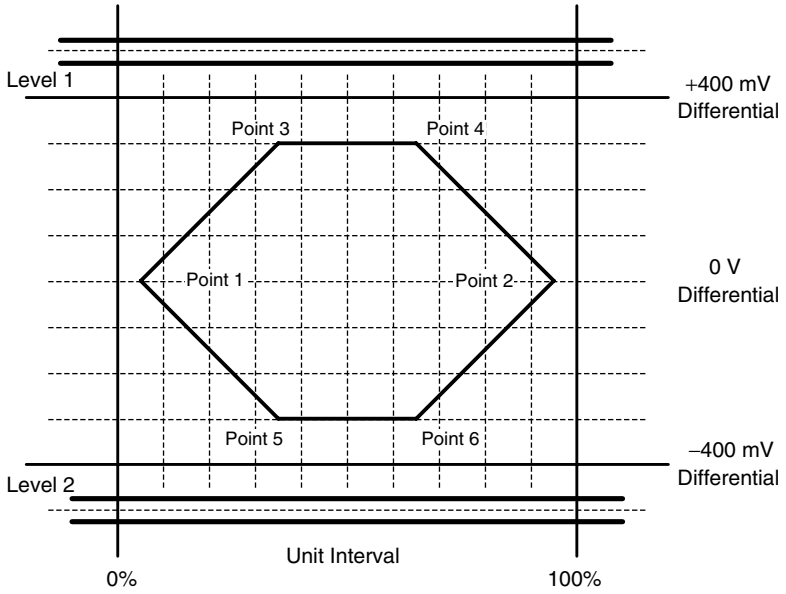
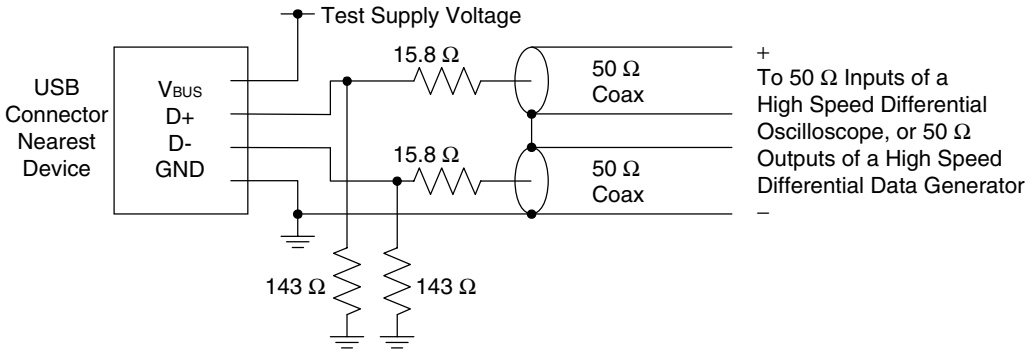
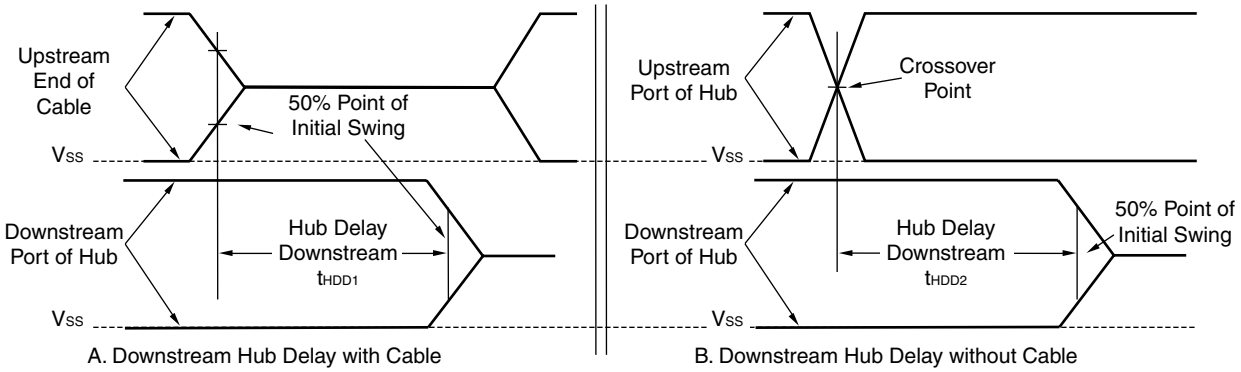


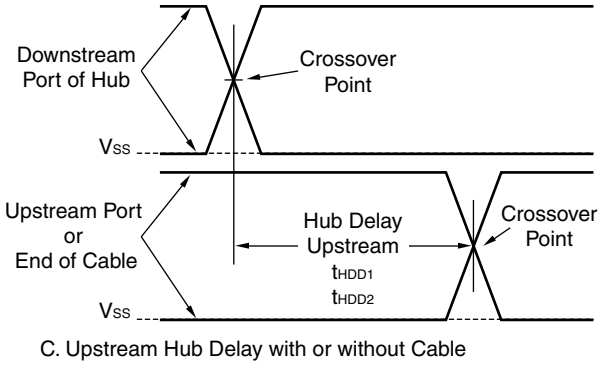
Figure 2-10. Transmitter Measurement Fixtures



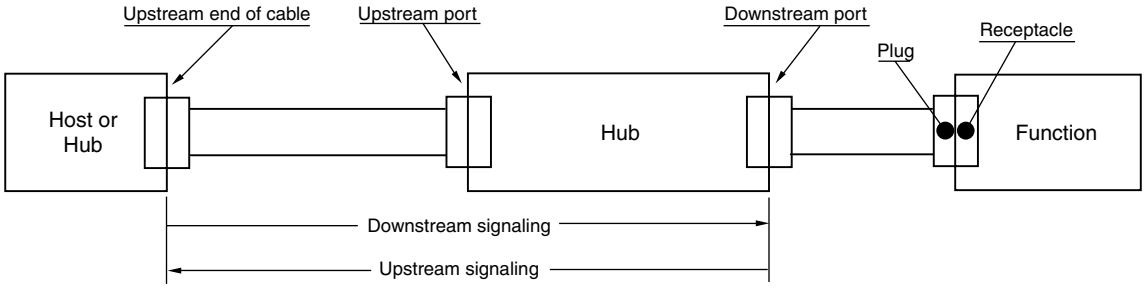
Timing Diagram

Figure 2-11. Hub Differential Delay, Differential Jitter, and SOP Distortion





C. Upstream Hub Delay with or without Cable



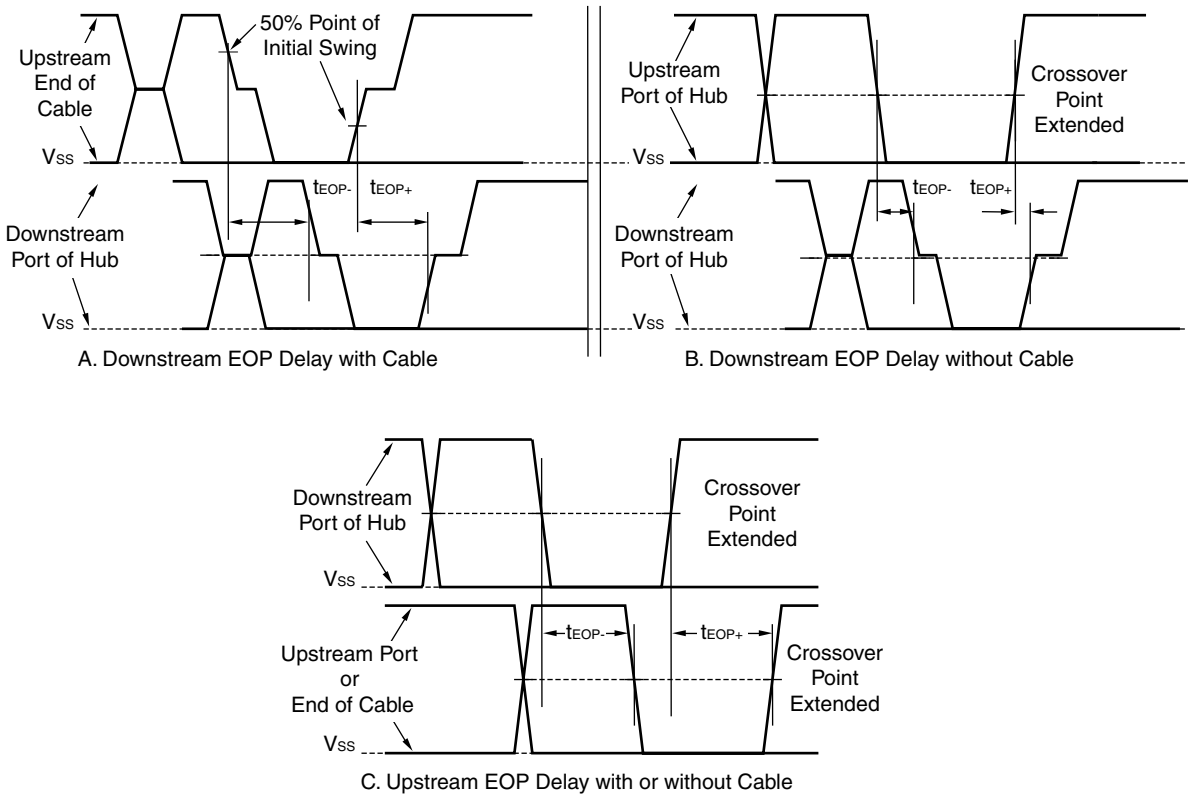
D. Measurement Points

Hub Differential Jitter:
$t_{HDJ1} = t_{HDDx}(J) - t_{HDDx}(K)$ or $t_{HDDx}(K) - t_{HDDx}(J)$ Consecutive Transitions
$t_{HDJ2} = t_{HDDx}(J) - t_{HDDx}(J)$ or $t_{HDDx}(K) - t_{HDDx}(K)$ Paired Transitions

Bit after SOP Width Distortion (same as data jitter for SOP and next J transition):
$t_{FSOP} = t_{HDDx}$(next J) $- t_{HDDx}$(SOP)

Low-speed timings are determined in the same way for:
t_{LHDD}, t_{LDHJ1}, t_{LDJH2}, t_{LUHJ1}, t_{LUJH2}, and t_{LSOP}

Figure 2-12. Hub EOP Delay and EOP Skew



EOP Delay:

$t_{FEOPD} = t_{EOPy} - t_{HDDx}$

(t_{EOPy} means that this equation applies to t_{EOP-} and t_{EOP+})

EOP Skew:

$t_{FHESK} = t_{EOP+} - t_{EOP-}$

Low-speed timings are determined in the same way for:

t_{LEOPD} and t_{LHESK}

Figure 2-13. USB Differential Data Jitter for Low-/full-speed

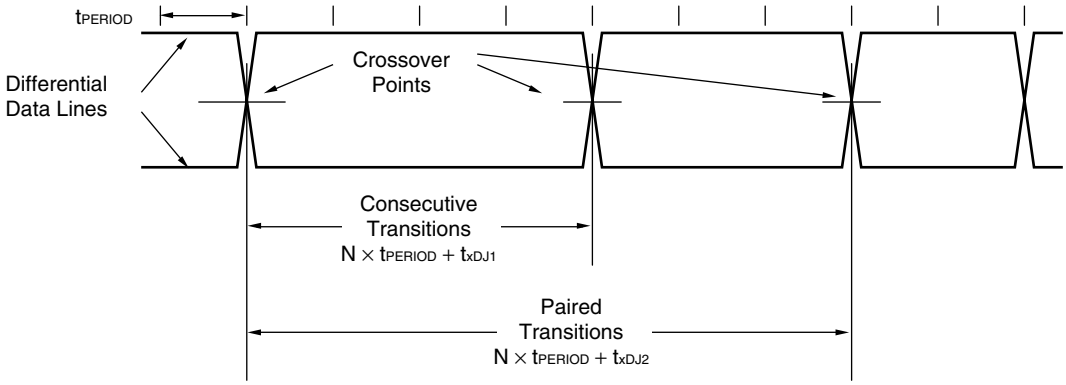


Figure 2-14. USB Differential-to-EOP Transition Skew and EOP Width for Low-/full-speed

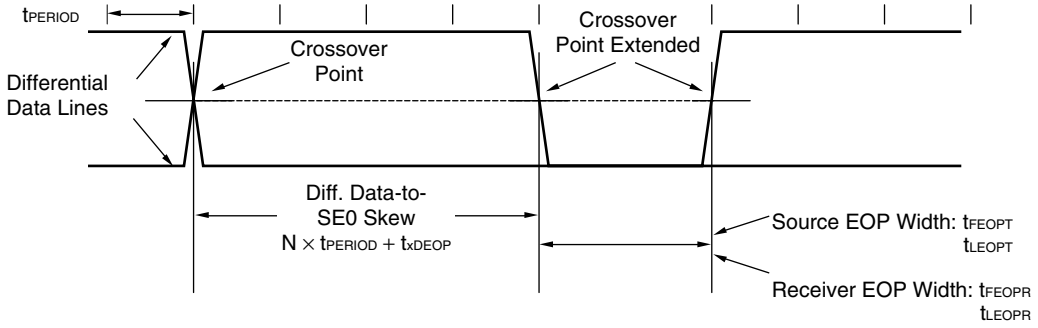


Figure 2-15. USB Receiver Jitter Tolerance for Low-/full-speed

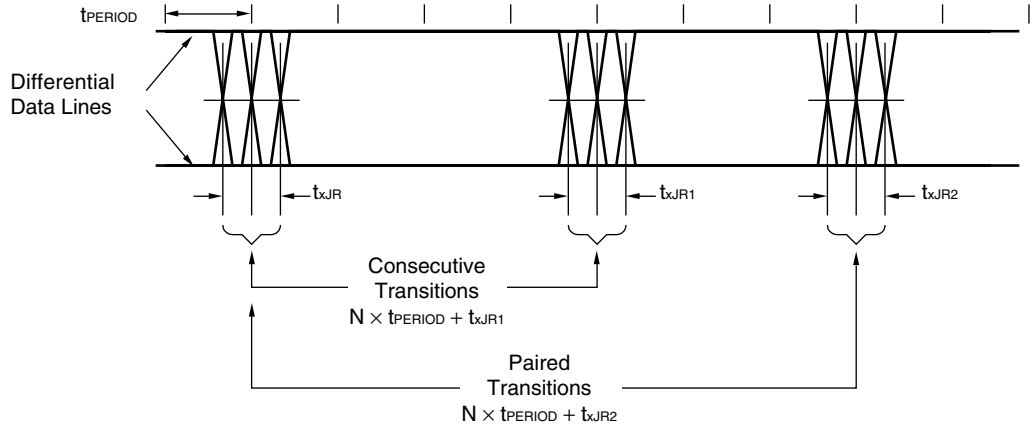


Figure 2-16. Low-/full-speed Disconnect Detection

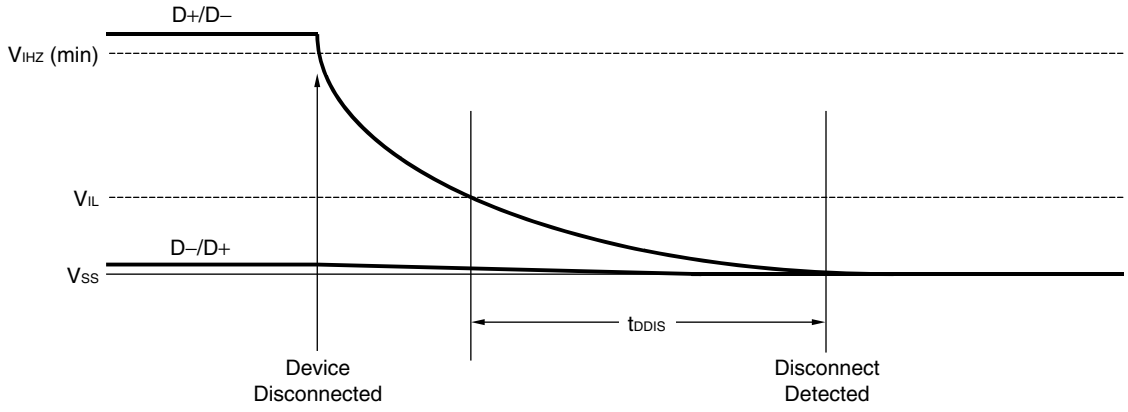


Figure 2-17. Full-/high-speed Device Connect Detection

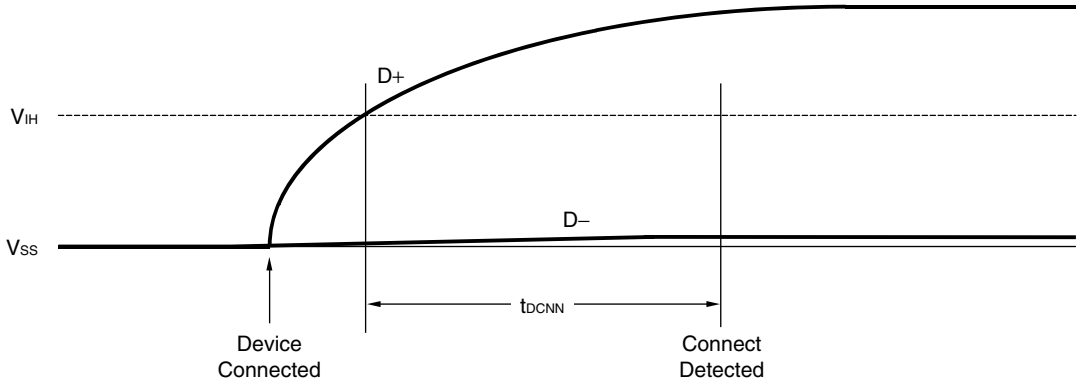
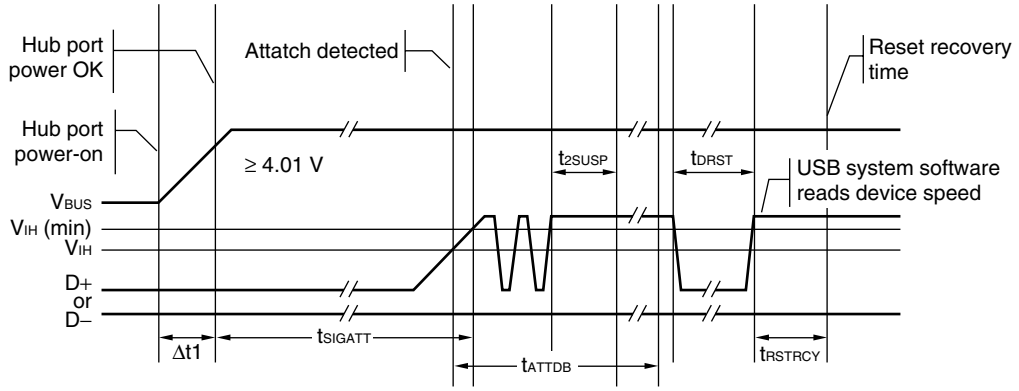


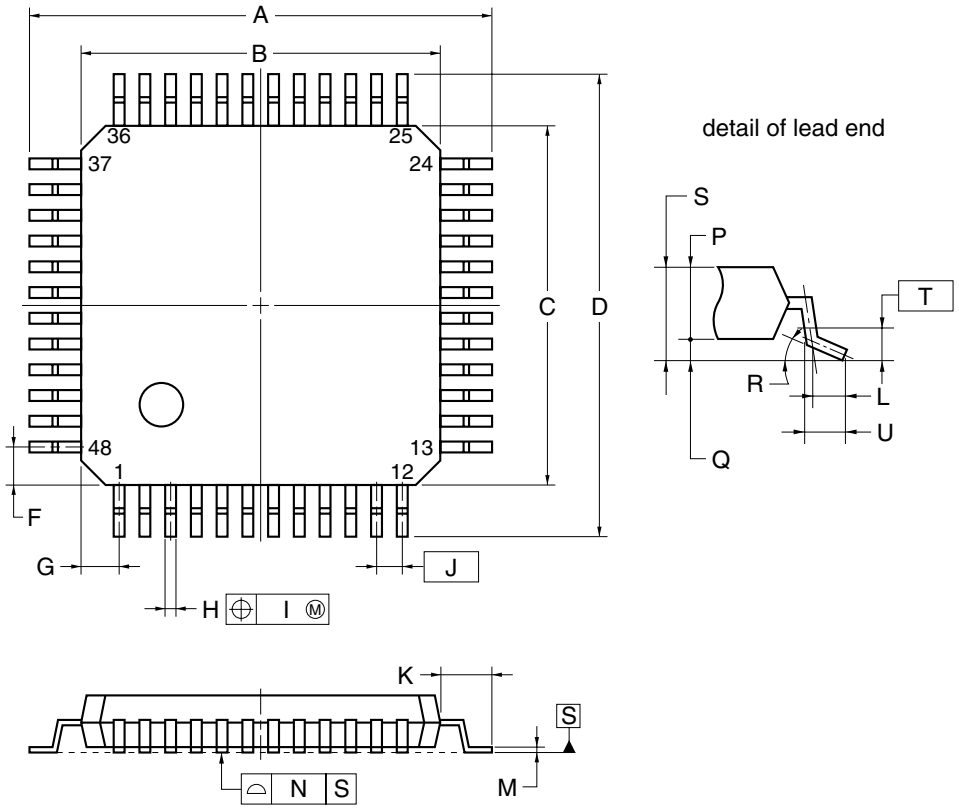
Figure 2-18. Power-on and Connection Events Timing



3. PACKAGE DRAWINGS

• **μPD720114GA-9EU-A**

48-PIN PLASTIC TQFP (FINE PITCH) (7x7)



NOTE

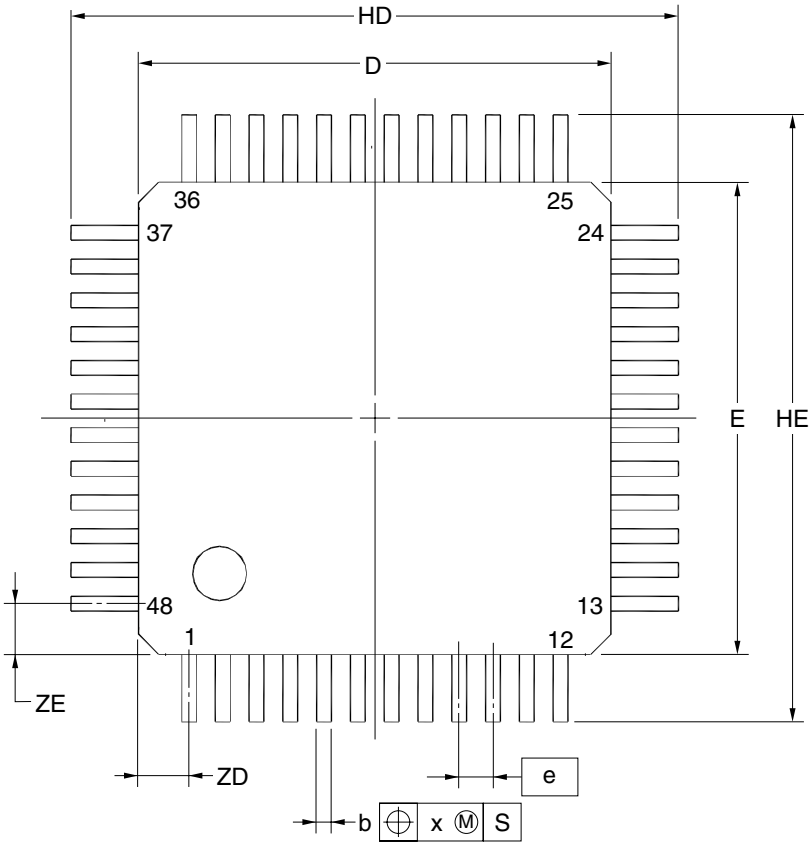
Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.0±0.2
B	7.0±0.2
C	7.0±0.2
D	9.0±0.2
F	0.75
G	0.75
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.0±0.1
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.27 MAX.
T	0.25 (T.P.)
U	0.6±0.15

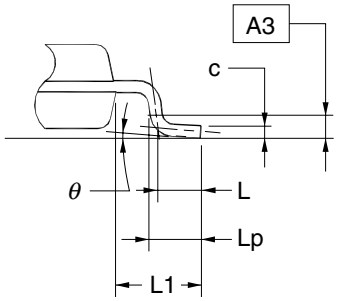
P48GA-50-9EU-1

• μPD720114GA-YEU-A

48-PIN PLASTIC TQFP (FINE PITCH)(7x7)



detail of lead end



(UNIT:mm)

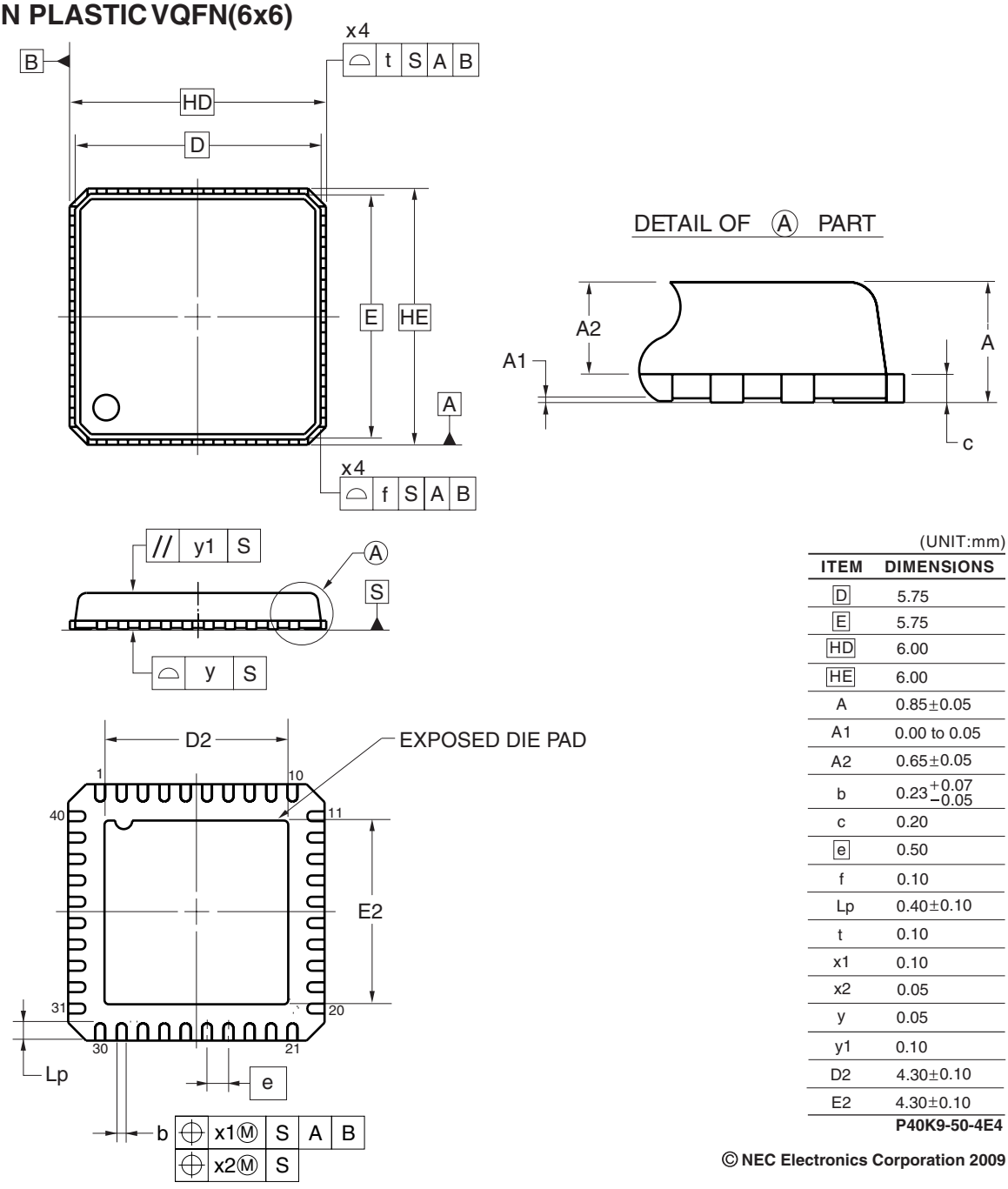
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.20 MAX.
A1	0.10±0.05
A2	1.00±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

P48GA-50-YEU

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

<R> • **μPD720114K9-4E4-A**

40-PIN PLASTIC VQFN(6x6)



(UNIT:mm)

ITEM	DIMENSIONS
D	5.75
E	5.75
HD	6.00
HE	6.00
A	0.85±0.05
A1	0.00 to 0.05
A2	0.65±0.05
b	$0.23^{+0.07}_{-0.05}$
c	0.20
e	0.50
f	0.10
Lp	0.40±0.10
t	0.10
x1	0.10
x2	0.05
y	0.05
y1	0.10
D2	4.30±0.10
E2	4.30±0.10

P40K9-50-4E4

4. RECOMMENDED SOLDERING CONDITIONS

The μPD720114 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

- μPD720114GA-9EU-A: 48-pin plastic TQFP (Fine pitch) (7 × 7)
- μPD720114GA-YEU-A: 48-pin plastic TQFP (Fine pitch) (7 × 7)

<R> • μPD720114K9-4E4-A: 40-pin plastic QFN (6 × 6)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Peak package's surface temperature: 260 °C, Reflow time: 60 seconds or less (220 °C or higher), Maximum allowable number of reflow processes: 3, Exposure limit Note: 7 days (10 to 72 hours pre-backing is required at 125C° afterwards), Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR60-107-3
Partial heating method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (per each side of the device) , Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.	–

Note The Maximum number of days during which the product can be stored at a temperature of 5 to 25°C and a relative humidity of 20 to 65% after dry-pack package is opened.

[MEMO]

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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